153 Ball eMMC DM9x Datasheet

(SQF-MM5xx-xxxGDM9x)

CONTENTS

Revision History

Rev.	Date	History
0.1	2021/11/5	Draft
0.2	2021/12/17	Added TBW data
0.3	2021/12/23	Added Consumption
0.4	2023/6/5	Added 8~32GB sTLC part number and spec.
0.5	2023/6/13	Added manufacturer part number information

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1. Overview

Advantech SQF eMMC products follow the JEDEC eMMC 5.1 standard. It is an ideal universal storage solution for many electronic devices, including smartphones, tablets, PDAs, eBook readers, digital cameras, recorders, MP3, MP4 players, electronic learning products, digital TVs and set-top boxes. eMMC encloses the BiCS5 (3D TLC) NAND and eMMC controller inside as one JEDEC standard package, providing a standard interface to the host. The eMMC controller directly manages NAND flash, including ECC, wear-leveling, IOPS optimization and read sensing.

Grade	Capacity	NAND Flash Type	Package	Operating Voltage	Package Size (mm)
Industrial	64 GB	3D TLC BiCS5 TLC	FBGA153	V_{CC}=3.3V, V_{CCQ}=3.3/1.8V	11.5 x 13.0 x 1.0 mm
	128 GB	3D TLC BiCS5 TLC			
	256 GB	3D TLC BiCS5 TLC			

Grade	Capacity	NAND Flash Type	Package	Operating Voltage	Package Size (mm)
Industrial	8 GB	3D TLC BiCS5 sTLC	FBGA153	V_{CC}=3.3V, V_{CCQ}=3.3/1.8V	11.5 x 13.0 x 1.0 mm
	16 GB	3D TLC BiCS5 sTLC			
	32 GB	3D TLC BiCS5 sTLC			

2. Features

- Packaged NAND flash memory with eMMC 5.1 interface
- Compliant with eMMC Specification Ver. 4.4, 4.41, 4.5, 4.51, 5.0, 5.1
- Bus mode
  - High-speed eMMC protocol
  - Clock frequency: 0-200MHz.
  - Ten-wire bus (clock, 1-bit command, 8-bit data bus) and a hardware reset.
- Supports three different data bus widths: 1 bit(default), 4 bits, 8 bits
  - Data transfer rate: up to 52Mbyte/s (using 8 parallel data lines at 52 MHz)
  - Single data rate: up to 200Mbyte/s @ 200MHz
  - Dual data rate: up to 400Mbyte/s @ 200MHz
- Operating voltage range:
  - VCCQ = 1.8 V/3.3V
  - VCC = 3.3 V
- Error free memory access
  - Internal error correction code (ECC) to protect data communication
  - Internal enhanced data management algorithm
  - Solid protection of sudden power failure safe-update operations for data content
- Security
  - Support secure erase/trim commands
  - Enhanced write Protection with permanent and partial protection options
- Quality
  - RoHS compliant
- Supports Field Firmware Update(FFU)
- Enhanced Device Life time
- Support Pre EOL information
- Optimal Size
- Supports Production State Awareness
- Supports Power Off Notification for Sleep
- Supports HS400
- Temperature Ranges
  - Commercial Temperature
    - ◆ -25℃ to 85℃ for operating
    - ◆ -40℃ to 85℃ for storage
- Weight: 0.2 (g)

3. Specification Table

3.1 Performance

Products		Typical value	
		Read Sequential (MB/s)	Write Sequential (MB/s)
3D TLC (BiCS5)	64GB	315	215
	128GB	315	225
	256GB	315	240
3D sTLC (BiCS5)	8 GB	315	215
	16 GB	315	215
	32 GB	315	225
	64 GB	315	240

Note 1: Values given for an 8-bit bus width, running HS400 mode from ADVANTECH proprietary tool, VCC=3.3V, VCCQ=1.8V.
Note 2: Performance numbers might be subject to changes without notice.

3.2 Power Consumption

Products		Read (mA)		Write (mA)		Standby (mA)	
		$V_{CCQ(1.8V)}$	$V_{CC(3.3V)}$	$V_{CCQ(1.8V)}$	$V_{CC(3.3V)}$	V_{CCQ}	V_{CC}
3D TLC (BiCS5)	64GB	155	100	70	65	0.15	0.06
	128GB	155	105	70	105	0.15	0.07
	256GB	155	110	80	165	0.15	0.09
3D sTLC (BiCS5)	8 GB	155	100	70	65	0.15	0.06
	16 GB	155	100	70	65	0.15	0.06
	32 GB	155	105	70	105	0.15	0.07
	64 GB	155	110	80	165	0.15	0.09

Note 1: Values given for an 8-bit bus width, a clock frequency of 200MHz DDR mode, VCC= 3.3V±5%, VCCQ=1.8V±5%
Note 2: Standby current is measured at VCC=3.3V±5%, 8-bit bus width without clock frequency.
Note 3: Current numbers might be subject to changes without notice.
Note 4: The measurement for max RMS current is done as average RMS current consumption over a period of 100ms.

3.3 Capacity according to partition

Products		Boot partition 1	Boot partition 2	RPMB
3D TLC (BiCS5)	64GB	4096 KB	4096 KB	4096 KB
	128GB	4096 KB	4096 KB	4096 KB
	256GB	4096 KB	4096 KB	4096 KB
3D sTLC (BiCS5)	8 GB	4096 KB	4096 KB	4096 KB
	16 GB	4096 KB	4096 KB	4096 KB
	32 GB	4096 KB	4096 KB	4096 KB
	64 GB	4096 KB	4096 KB	4096 KB

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3.4 Endurance

JEDEC defined an endurance rating TBW (TeraByte Written), following by the equation below, for indicating the number of terabytes a SSD can be written which is a measurement of SSDs' expected lifespan, represents the amount of data written to the device.

TBW = [(NAND Endurance) x (SSD Capacity)] / WAF

- **NAND Endurance**: Program / Erase cycle of a NAND flash.
  - 3D TLC (BiCS5): 3,000 cycles
  - 3D sTLC (BiCS5): 30,000 cycles
- **SSD Capacity**: SSD physical capacity in total of a SSD.
- **WAF**: Write Amplification Factor (WAF), as the equation shown below, is a numerical value representing the ratio between the amount of data that a SSD controller needs to write and the amount of data that the host's flash controller writes. A better WAF, which is near to 1, guarantees better endurance and lower frequency of data written to flash memory.

WAF = (Lifetime write to flash) / (Lifetime write to host)

Endurance measurement is based on JEDEC 219A client workload and verified with following workload conditions,

- PreCond%full = 100%
- Trim commands enabled
- Random data pattern.

Capacity	TBW
	3D TLC (BiCS5)
64 GB	56
128 GB	TBD
256 GB	TBD

Capacity	TBW
	3D sTLC (BiCS5)
8 GB	TBD
16 GB	TBD
32 GB	TBD
64 GB	TBD

3.5 User Density Size

Total user density depends on device type.

For example, 52MB in the SLC mode requires 104 MB in 3D TLC BiCS3 (2-bit). This results in decreasing.

Capacity	User Density Size (Bytes)
8 GB	7,818,182,656
16 GB	15,627,976,704
32 GB	31,264,342,016
64 GB	62,537,072,640
128 GB	125,074,145,280
256 GB	250,148,290,560

4. eMMC Device and System

4.1 eMMC System Overview

The eMMC specification covers the behavior of the interface and the device controller. As part of this specification the existence of a host controller and a memory storage array are implied but the operation of these pieces is not fully specified.

Advantech NAND Device consists of a single chip MMC controller and NAND flash memory module. The micro-controller interfaces with a host system allowing data to be written to and read from the NAND flash memory module. The controller allows the host to be independent from details of erasing and programming the flash memory.

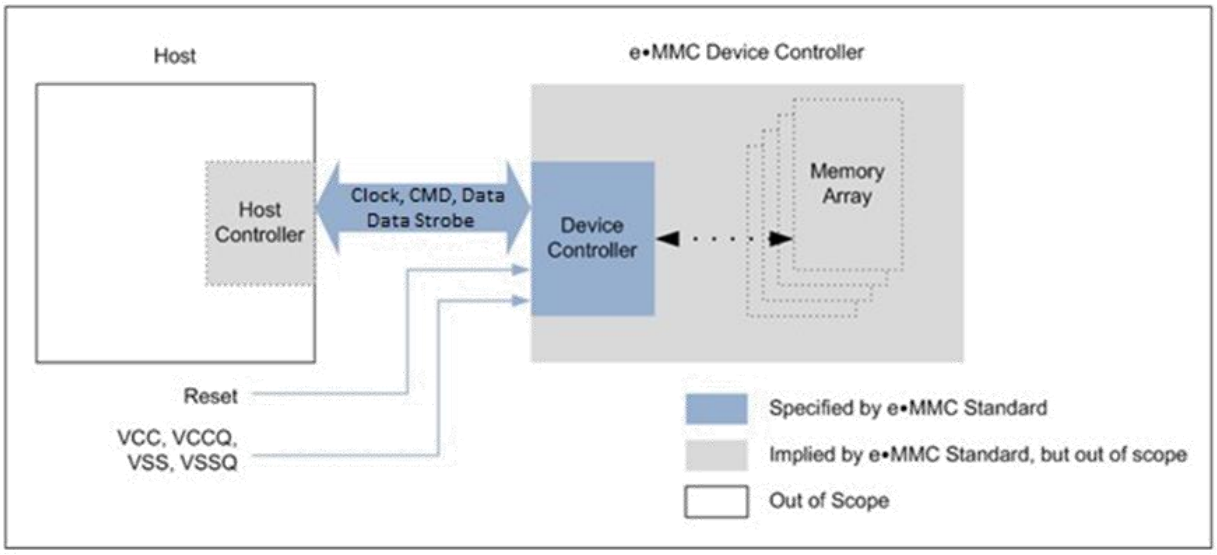


Figure 1– eMMC System Overview

4.2 Memory Addressing

Previous implementations of the eMMC specification are following byte addressing with 32-bit field. This addressing mechanism permitted for eMMC densities up to and including 2 GB.

To support larger density, the addressing mechanism was update to support sector addresses (512 B sectors). The sector addresses shall be used for all devices with capacity larger than 2 GB.

To determine the addressing mode, use the host should read bit [30:29] in the OCR register.

4.3 eMMC Device Overview

The eMMC device transfers data via a configurable number of data bus signals. The communication signals are:

4.3.1 Clock (CLK)

Each cycle of this signal directs a one-bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.

4.3.2 Data Strobe(DS)

This signal is generated by the device and used for output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output each cycle of this signal directs two bits transfer(2x) on the data - one bit for positive edge and the other bit for negative edge. For CRC status response output and CMD response output (enabled only HS400 enhanced strobe mode), the CRC status is latched on the positive edge only, and don't care on the negative edge.

4.3.3 Command (CMD)

This signal is a bidirectional command channel used for Device initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the eMMC host controller to the eMMC Device and responses are sent from the Device to the host.

4.3.4 Input/Outputs (DAT0-DAT7)

These are bidirectional data channels. The DAT signals operate in push-pull mode. Only the Device or the host is driving these signals at a time. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the eMMC host controller. The eMMC Device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the Device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode the Device disconnects the internal pull-ups of lines DAT1–DAT7.

Table 4– Communication Interface

Name	Type1	Description
CLK	I	Clock
DAT0	I/O/PP	Data
DAT1	I/O/PP	Data
DAT2	I/O/PP	Data
DAT3	I/O/PP	Data
DAT4	I/O/PP	Data
DAT5	I/O/PP	Data
DAT6	I/O/PP	Data
DAT7	I/O/PP	Data
CMD	I/O/PP/OD	Command/Response
RST_n	I	Hardware reset
VCC	S	Supply voltage for Core
VCCQ	S	Supply voltage for I/O
VSS	S	Supply voltage ground for Core
VSSQ	S	Supply voltage ground for I/O
DS	O/PP	Data strobe
Note1：I: input; O: output; PP: push-pull; OD: open-drain; NC: Not connected (or logical high); S: power supply.		

Table 5– eMMC Registers

Name	Width (Bytes)	Description	Implementation
CID	16	Device Identification number, an individual number for identification.	Mandatory
RCA	2	Relative Device Address is the Device system address, dynamically assigned by the host during initialization.	Mandatory
DSR	2	Driver Stage Register, to configure the Device's output drivers.	Optional
CSD	16	Device Specific Data, information about the Device operation conditions.	Mandatory
OCR	4	Operation Conditions Register. Used by a special broadcast command to identify the voltage type of the Device.	Mandatory
EXT_CSD	512	Extended Device Specific Data. Contains information about the Device capabilities and selected modes. Introduced in standard v4.0	Mandatory

The host may reset the device by:
- Switching the power supply off and back on. The device shall have its own power-on detection circuitry which puts the device into a defined state after the power-on Device.
- A reset signal
- By sending a special command

4.4 Bus Protocol

After a power-on reset, the host must initialize the device by a special message-based eMMC bus protocol. For more details, refer to section 5.3.1 of the JEDEC Standard Specification No.JESD84-B51.

4.5 Bus Speed Modes

eMMC defines several bus speed modes as shown in Table 6.

Table 6— Bus Speed Mode

Mode Name	Data Rate	IO Voltage	Bus Width	Frequency	Max Data Transfer (implies x8 bus width)
Backwards Compatibility with legacy MMC card	Single	3.3/1.8V	1, 4, 8	0-26MHz	26MB/s
High Speed SDR	Single	3.3/1.8V	4, 8	0-52MHz	52MB/s
High Speed DDR	Dual	3.3/1.8V	4, 8	0-52MHz	104MB/s
HS200	Single	1.8V	4, 8	0-200MHz	200MB/s
HS400	Dual	1.8V	8	0-200MHz	400MB/s

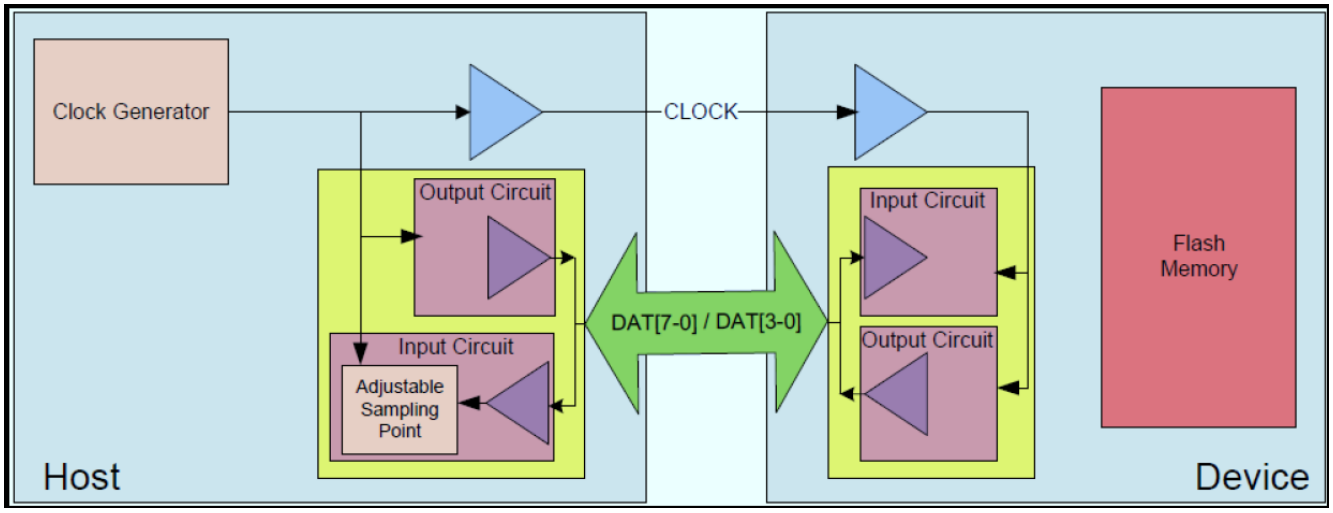
4.5.1 HS200 Bus Speed Mode

The HS200 mode offers the following features:
- SDR Data sampling method
- CLK frequency up to 200MHz Data rate – up to 200MB/s
- 8-bits bus width supported
- Single ended signaling with 4 selectable Drive Strength
- Signaling levels of 1.8V
- Tuning concept for Read Operations

4.5.2 HS200 System Block Diagram

Figure 2 shows a typical HS200 Host and Device system. The host has a clock generator, which supplies CLK to the Device. For write operations, clock and data direction are the same, write data can be transferred synchronous with CLK, regardless of transmission line delay. For read operations, clock and data direction are opposite; the read data received by Host is delayed by round-trip delay, output delay and latency of Host and Device. For reads, the Host needs to have an adjustable sampling point to reliably receive the incoming data.

Figure 2— System Block Diagram



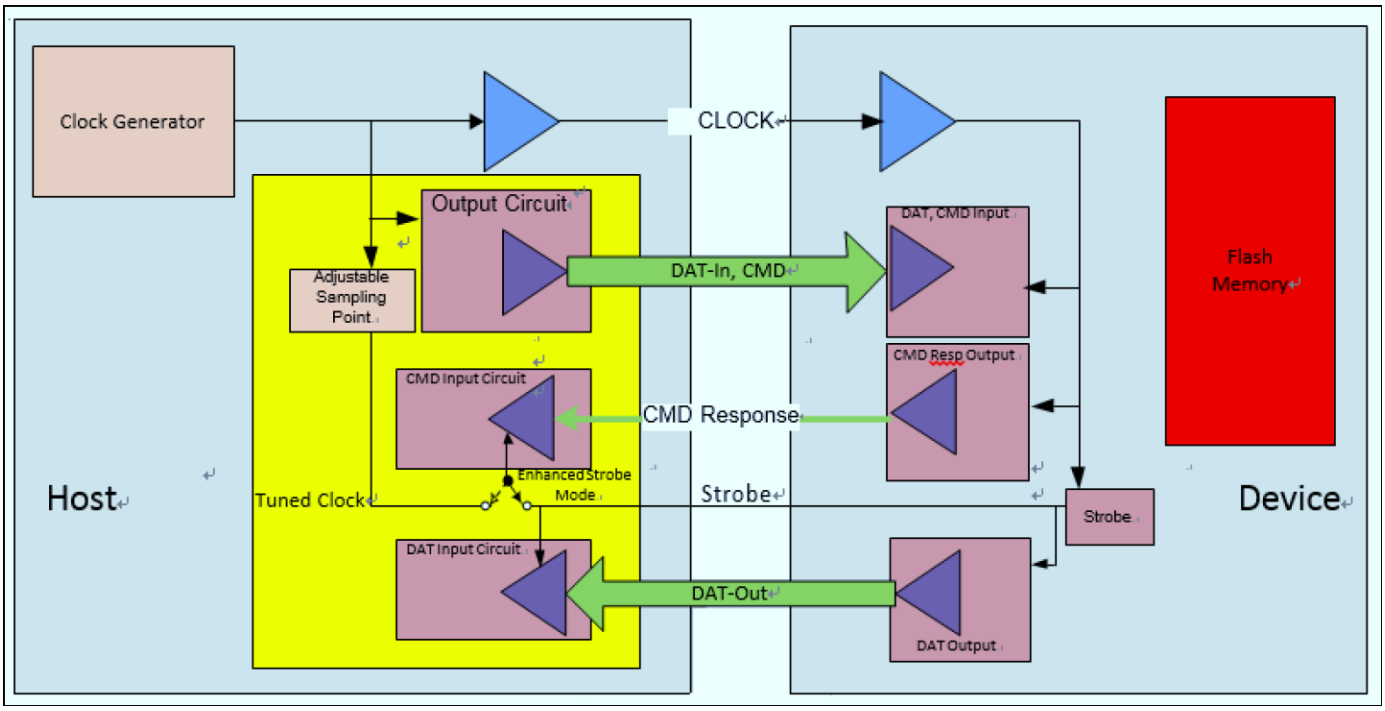
4.5.3 HS400 Bus Speed mode

The HS400 mode has the following features
- DDR Data sampling method
- CLK frequency up to 200MHz, Data rate is – up to 400MB/s
- Only 8-bit bus width supported
- Signaling levels of 1.8V
- Support up to 5 selective Drive Strength
- Data strobe signal is toggled only for Data out and CRC response

4.5.4 HS400 System Block Diagram

Figure 3 shows a typical HS400 Host and Device system. The host has a clock generator, which supplies CLK to the Device. For read operations, Data Strobe is generated by device output circuit. Host receives the data which is aligned to the edge of Data Strobe.

Figure 3- HS400 Host and Device block diagram



5. eMMC Functional Description

5.1 eMMC Overview

All communication between host and device are controlled by the host (main chip). The host sends a command, which results in a device response. For more details, refer to section 6.1 of the JEDEC Standard Specification No.JESD84-B51.

Five operation modes are defined for the eMMC system:

- Boot operation mode
- Device identification mode
- Interrupt mode
- Data transfer mode
- Inactive mode

5.2 Boot Operation Mode

In boot operation mode, the master (eMMC host) can read boot data from the slave (eMMC device) by keeping CMD line low or sending CMD0 with argument + 0xFFFFFFFA, before issuing CMD1. The data can be read from either boot area or user area depending on register setting. For more details, refer to section 6.3 of the JEDEC Standard Specification No.JESD84-B51.

5.3 Device Identification Mode

While in device identification mode the host resets the device, validates operation voltage range and access mode, identifies the device and assigns a Relative device Address (RCA) to the device on the bus. All data communication in the Device Identification Mode uses the command line (CMD) only. For more details, refer to section 6.4 of the JEDEC Standard Specification No.JESD84-B51.

5.4 Interrupt Mode

The interrupt mode on the eMMC system enables the master (eMMC host) to grant the transmission allowance to the slaves (Device) simultaneously. This mode reduces the polling load for the host and hence, the power consumption of the system, while maintaining adequate responsiveness of the host to a Device request for service. Supporting eMMC interrupt mode is an option, both for the host and the Device. For more details, refer to section 6.5 of the JEDEC Standard Specification No.JESD84-B51.

5.5 Data Transfer Mode

When the Device is in Stand-by State, communication over the CMD and DAT lines will be performed in push-pull mode. For more details, refer to section 6.6 of the JEDEC Standard Specification No.JESD84-B51.

5.6 Inactive Mode

The device will enter inactive mode if either the device operating voltage range or access mode is not valid. The device can also enter inactive mode with GO_INACTIVE_STATE command (CMD15). The device will reset to Pre-idle state with power cycle. For more details, refer to section 6.1 of the JEDEC Standard Specification No.JESD84-B51.

5.7 H/W Reset Operation

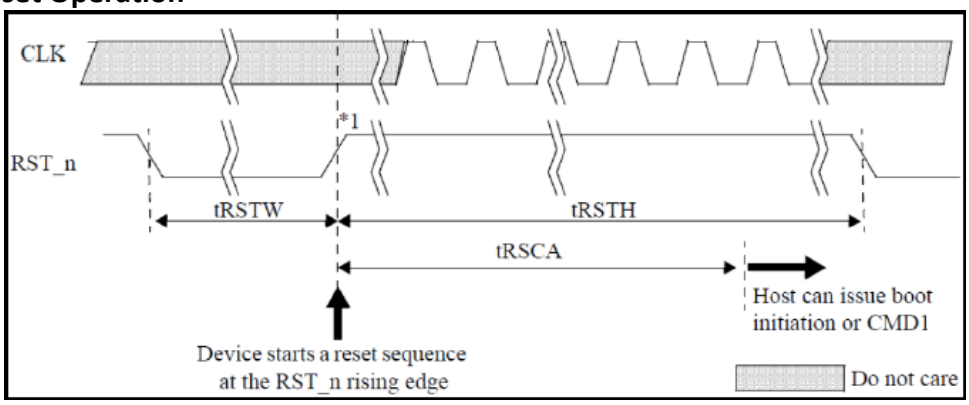


Figure 4– H/W Reset Waveform

Note1: Device will detect the rising edge of RST_n signal to trigger internal reset sequence

Table 7– H/W Reset Timing Parameters

Symbol	Comment	Min	Max	Unit
tRSTW	RST_n pulse width	1		[us]
tRSCA	RST_n to Command time	200[1]		[us]
tRSTH	RST_n high period (interval time)	1		[us]
Note1：74 cycles of clock signal required before issuing CMD1 or CMD0 with argument 0xFFFFFFFA				

5.8 Noise Filtering Timing for H/W Reset

Device must filter out 5ns or less pulse width for noise immunity

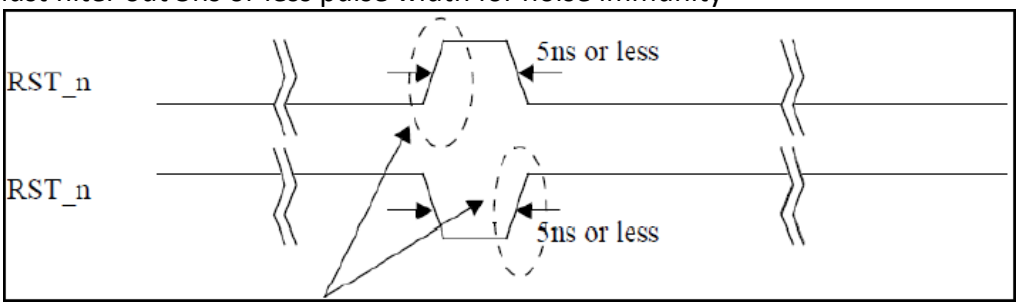


Figure 5– Noise Filtering Timing for H/W Reset

Device must not detect these rising edge.
Device must not detect 5ns or less of positive or negative RST_n pulse.
Device must detect more than or equal to 1us of positive or negative RST_n pulse width.

5.9 Field Firmware Update (FFU)

Field Firmware Updates (FFU) enables features enhancement in the field. Using this mechanism the host downloads a new version of the firmware to the eMMC device and, following a successful download, instructs the eMMC device to install the new downloaded firmware into the device.

In order to start the FFU process the host first checks if the eMMC device supports FFU capabilities by reading SUPPPORTED_MODES and FW_CONFIG fields in the EXT_CSD. If the eMMC device supports the FFU feature the host may start the FFU process. The FFU process starts by switching to FFU Mode in MODE_CONFIG field in the EXT_CSD. In FFU Mode host should use closed-ended or open ended commands for downloading the new firmware and reading vendor proprietary data. In this mode, the host should set the argument of these commands to be as defined in FFU_ARG field. In case these commands have a different argument the device behavior is not defined and the FFU process may fail. The host should set Block Length to be DATA_SECTOR_SIZE. Downloaded firmware bundle must be DATA_SECTOR_SIZE size aligned (internal padding of the bundle might be required).Once in FFU Mode the host may send the new firmware bundle to the device using one or more write commands.

The host could regain regular functionality of write and read commands by setting MODE_CONFIG field in the EXT_CSD back to Normal state. Switching out of FFU Mode may abort the firmware download operation. When host switched back to FFU Mode, the host should check the FFU Status to get indication about the number of sectors which were downloaded successfully by reading the NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED in the extended CSD. In case the number of sectors which were downloaded successfully is zero the host should re-start downloading the new firmware bundle from its first sector. In case the number of sectors which were downloaded successfully is positive the host should continue the download from the next sector, which would resume the firmware download operation.

In case MODE_OPERATION_CODES field is not supported by the device the host sets to NORMAL state and initiates a CMD0/HW_Reset/Power cycle to install the new firmware. In such case the device doesn’t need to use NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED.

In both cases occurrence of a CMD0/HW_Reset/Power occurred before the host successfully downloaded the new firmware bundle to the device may cause the firmware download process to be aborted.

5.10 Power off Notification for sleep

The host should notify the device before it powers the device off. This allows the device to better prepare itself for being powered off. Power the device off means to turn off all its power supplies. In particular, the host should issue a power off notification (POWER_OFF_LONG, POWER_OFF_SHORT) if it intends to turn off both VCC and VCCQ power I or it may use to a power off notification (SLEEP_NOTIFICATION) if it intends to turn-off VCC after moving the device to Sleep state.

To indicate to the device that power off notification is supported by the host, a supporting host shall first set the POWER_OFF_NOTIFICATION byte in EXT_CSD [34] to POWERED_ON (0x01). To execute a power off, before powering the device down the host will changes the value to either

POWER_OFF_SHORT (0x02) or POWER_OFF_LONG (0x03). Host should waits for the busy line to be de-asserted. Once the setting has changed to either 0x02 or 0x03, host may safely power off the device.

The host may issue SLEEP_AWAKE (CMD5) to enter or to exit from Sleep state if POWER_OFF_NOTIFICATION byte is set to POWERED_ON. Before moving to Standby state and then to Sleep state, the host sets POWER_OFF_NOTIFICATION to SLEEP_NOTIFICATION and waits for the DAT0 line de-assertion. While in Sleep (slp) state VCC (Memory supply) may be turned off as defined in 4.1.6. Removing power supplies other than VCC while the device is in the Sleep (slp) state may result in undefined device behavior. Before removing all power supplies, the host should transition the device out of Sleep (slp) state back to Transfer state using CMD5 and CMD7 and then execute a power off notification setting POWER_OFF_NOTIFICATION byte to either POWER_OFF_SHORT or POWER_OFF_LONG.

If host continues to send commands to the device after switching to the power off setting (POWER_OFF_LONG, POWER_OFF_SHORT or SLEEP_NOTIFICATION) or performs HPI during its busy condition, the device shall restore the POWER_OFF_NOTIFICATION byte to POWERED_ON.
If host tries to change POWER_OFF_NOTIFICATION to 0x00 after writing another value there, a SWITCH_ERROR is generated.

The difference between the two power-off modes is how urgent the host wants to turn power off. The device should respond to POWER_OFF_SHORT quickly under the generic CMD6 timeout. If more time is acceptable, POWER_OFF_LONG may be used and the device shall respond to it within the POWER_OFF_LONG_TIME timeout.

While POWER_OFF_NOTIFICATION is set to POWERED_ON, the device expects the host to host shall:

- Keep the device power supplies alive (both VCC and VCCQ) and in their active mode
- Not power off the device intentionally before changing POWER_OFF_NOTIFICATION to either POWER_OFF_LONG or POWER_OFF_SHORT
- Not power off VCC intentionally before changing POWER_OFF_NOTIFICATION to SLEEP_NOTIFICATION and before moving the device to Sleep state

Before moving to Sleep state hosts may set the POWER_OFF_NOTIFICATION byte to SLEEP_NOTIFICATION (0x04) if aware that the device is capable of autonomously initiating background operations for possible performance improvements. Host should wait for the busy line to be de-asserted. Busy line may be asserted up the period defined in SLEEP_NOTIFICATION_TIME byte in EXT_CSD [216]. Once the setting has changed to 0x04 host may set the device into Sleep mode (CMD7+CMD5). After getting out from Sleep the POWER_OFF_NOTIFICATION byte will restore its value to POWERED_ON. HPI may interrupt the SLEEP_NOTIFICATION operation. In that case POWER_OFF_NOTIFICATION byte will restore to POWERED_ON.

5.11 Enhanced User Data Area

eMMC supports Enhanced User Data Area feature which allows the User Data Area of eMMC to be configured as SLC Mode. Therefore when host set the Enhanced User Data Area, the area will occupy double size of original set up size. The Max Enhanced User Data Area size is defined as - (MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512 KBytes). The Enhanced use data area size is defined as - (ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512 KBytes). The host shall follow the flow chart of JEDEC spec for configuring the parameters of General Purpose Area Partitions and Enhanced User Data Area.

6. Register Settings

Within the Device interface six registers are defined: OCR, CID, CSD, EXT_CSD, RCA and DSR. These can be accessed only by corresponding commands (see Section 6.10 of JESD84-B51).

6.1 OCR Register

The 32-bit operation conditions register (OCR) stores the VDD voltage profile of the Device and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the Device power up procedure has been finished. The OCR register shall be implemented by all Devices.

6.2 CID Register

The Card Identification (CID) register is 128 bits wide. It contains the Device identification information used during the Device identification phase (eMMC protocol). For details, refer to JEDEC Standard Specification.

6.3 CSD Register

The Card-Specific Data (CSD) register provides information on how to access the contents stored in eMMC. The CSD registers are used to define the error correction type, maximum data access time, data transfer speed, data format…etc. For details, refer to section 7.3 of the JEDEC Standard Specification No.JESD84-B51.

6.4 Extended CSD Register

The Extended CSD register defines the Device properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the Device is working in. These modes can be changed by the host by means of the SWITCH command.

6.5 RCA Register

The writable 16-bit Relative Device Address (RCA) register carries the Device address assigned by the host during the Device identification. This address is used for the addressed host-Device communication after the Device identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all Devices into the Stand-by State with CMD7.

6.6 DSR Register

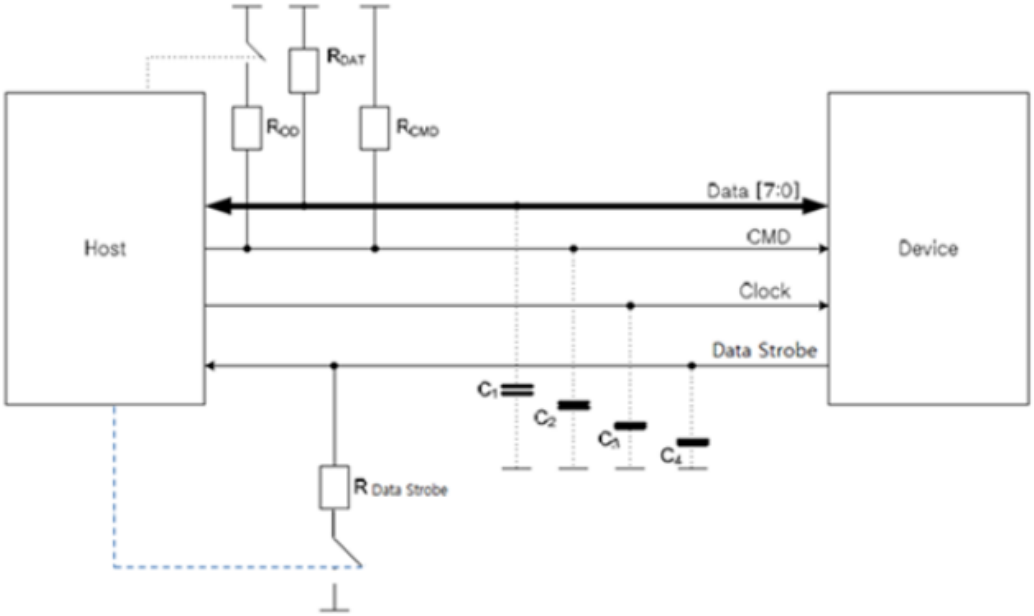
The 16-bit driver stage register (DSR) is described in detail in Section 7.6 of the JEDEC Standard Specification No.JESD84-B51. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of Devices). The CSD register carries the information about the DSR register usage.

7. The eMMC bus

The eMMC bus has ten communication lines and three supply lines:

- CMD: Command is a bidirectional signal. The host and Device drivers are operating in two modes, open drain and push/pull.
- DAT0-7: Data lines are bidirectional signals. Host and Device drivers are operating in push-pull mode
- CLK: Clock is a host to Device signal. CLK operates in push-pull mode
- Data Strobe: Data Strobe is a Device to host signal. Data Strobe operates in push-pull mode.

Figure 6– Bus Circuitry Diagram



The ROD is switched on and off by the host synchronously to the open-drain and push-pull mode transitions. The host does not have to have open drain drivers, but must recognize this mode to switch on the ROD. RDAT and RCMD are pull-up resistors protecting the CMD and the DAT lines against bus floating device when all device drivers are in a high-impedance mode.

A constant current source can replace the ROD by achieving a better performance (constant slopes for the signal rising and falling edges). If the host does not allow the switchable ROD implementation, a fixed RCMD can be used).Consequently the maximum operating frequency in the open drain mode has to be reduced if the used RCMD value is higher than the minimal one given in.

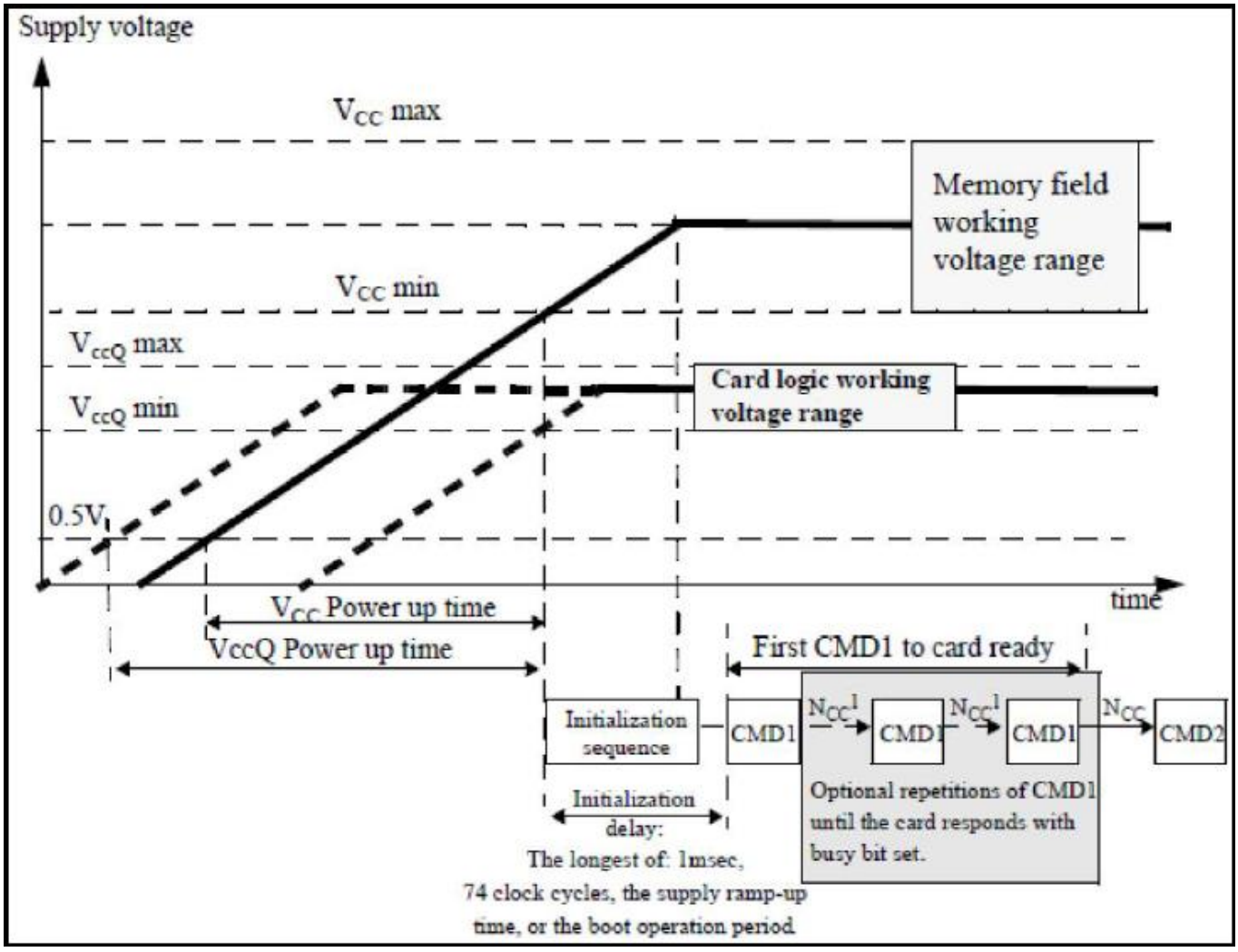
$R_{Data\ strobe}$ is pull-down resistor used in HS400 device.

7.1 Power-up

7.1.1 eMMC power-up

An eMMC bus power-up is handled locally in each device and in the bus master. Figure7 shows the power-up sequence and is followed by specific instructions regarding the power-up sequence. Refer to section 10.1 of the JEDEC Standard Specification No.JESD84-B51 for specific instructions regarding the power-up sequence.

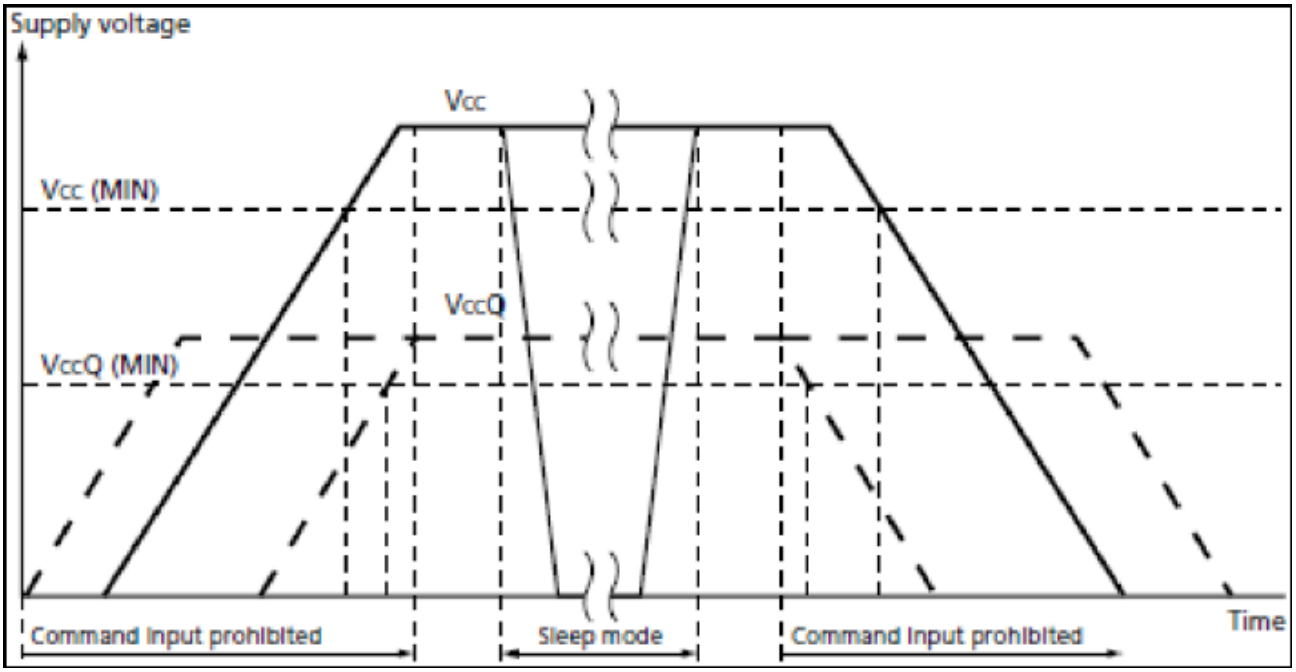
Figure 7 – eMMC Power-up Diagram



7.1.2 eMMC Power Cycling

The master can execute any sequence of VCC and VCCQ power-up/power-down. However, the master must not issue any commands until VCC and VCCQ are stable within each operating voltage range. After the slave enters sleep mode, the master can power-down VCC to reduce power consumption. It is necessary for the slave to be ramped up to VCC before the host issues CMD5 (SLEEP_AWAKE) to wake the slave unit. For more information about power cycling see Section 10.1.3 of the JEDEC Standard Specification No.JESD84-B51.

Figure 8– The eMMC Power Cycle



7.1.3 Power Cycle Requirements

As part of a power cycle, the host shall hold both the VCC and VCCQ voltage levels below 100mV for a minimum time of 1ms.

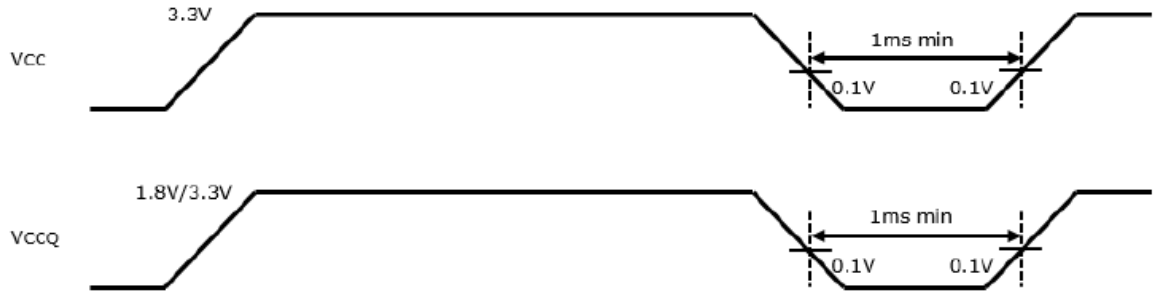


Figure-9. VCC, VCCQ Power Cycle Requirements

7.2 Bus Operating Conditions

Parameter	Symbol	Min	Max.	Unit	Remark
Peak voltage on all lines		-0.5	VCCQ + 0.5	V	
All Inputs					
Input Leakage Current (before initialization sequence [1] and/or the internal pull up resistors connected)		-100	100	µA	
Input Leakage Current (after initialization sequence and the internal pull up resistors disconnected)		-2	2	µA	
All Outputs					
Output Leakage Current (before initialization sequence)		-100	100	µA	
Output Leakage Current (after initialization sequence) [2]		-2	2	µA	
Note1：Initialization sequence is defined in section 10.1 Note2：DS (Data strobe) pin is excluded.					

Table 9– General Operating Conditions

7.2.1 Power supply: eMMC

In the eMMC, VCC is used for the NAND flash device and its interface voltage; VCCQ is for the controller and the MMC interface voltage as shown in Figure 9. The core regulator is optional and only required when internal core logic voltage is regulated from VCCQ. A CReg capacitor must be connected to the VDDi terminal to stabilize regulator output on the system.

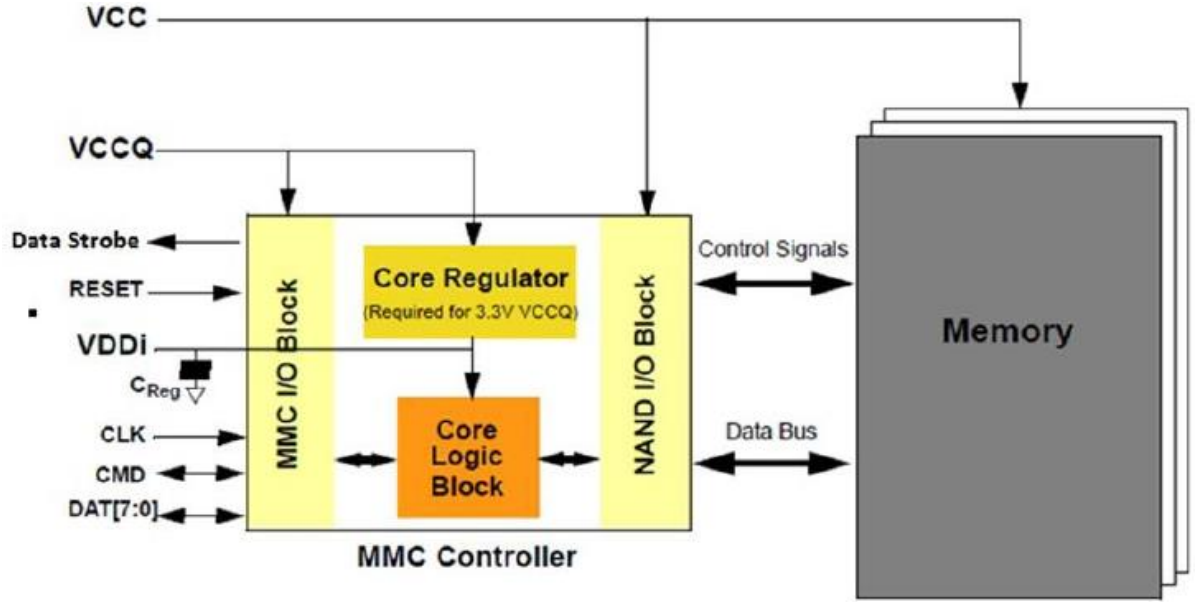


Figure 10– eMMC Internal Power Diagram

7.2.2 eMMC Power Supply Voltage

The eMMC supports one or more combinations of VCC and VCCQ as shown in Table 9. The VCCQ must be defined at equal to or less than VCC.

AC noise Criteria:

AC noise on the supply voltage shall not exceed ± 3%. 10 kHz to 800 MHz AC and DC noise together shall stay within the Min-Max range specified in this table 10.

Parameter	Symbol	MIN	MAX	Unit	Remarks
Supply voltage (NAND)	VCC	2.7	3.6	V	
Supply voltage (I/O)	VCCQ	2.7	3.6	V	
		1.7	1.95	V	
Supply power-up for 3.3V	tPRUH	0.036	35	ms	
Supply power-up for 1.8V	tPRUL	0.018	25	ms	
NOTE: Power noise on the supply voltage shall not exceed +/-3%.					

Table 10– eMMC Operating Voltage

The eMMC must support at least one of the valid voltage configurations, and can optionally support all valid voltage configurations (see Table).

		V_{CCQ}	
		1.7V–1.95V	2.7V–3.6V[1]
Vcc	2.7V-3.6V	Valid	Valid
Note1：V_{CCQ} (I/O) 3.3 volt range is not supported in HS200 /HS400 devices			

Table 11 – eMMC Voltage Combinations

7.2.3 Bus Signal Line Load

The total capacitance CL of each line of the eMMC bus is the sum of the bus master capacitance CHOST, the bus capacitance CBUS itself and the capacitance CDEVICE of eMMC connected to this line:

CL = CHOST + CBUS + CDEVICE

The sum of the host and bus capacitances must be under 20pF.

Parameter	Symbol	Min	Max	Typ	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7	50	10	Kohm	to prevent bus floating
Pull-up resistance for DAT0–7	R_{DAT}	10	50	10	Kohm	to prevent bus floating
Pull-up resistance for RST_n	R_{RST_n}	4.7	50	10	Kohm	It is not necessary to put pull-up resistance on RST_n (H/W rest) line if host does not use H/W reset. (Extended CSD register [162] = 0 b)
Bus signal line capacitance	CL		30	30	pF	Single Device
Single Device capacitance	C_{BGA}		6	6	pF	
Maximum signal line inductance			16	16	nH	
Impedance on CLK / CMD / DAT0~7		45	55	50	ohm	Impedance match
Serial's resistance on CLK line	SR_{CLK}	0	47	0	ohm	
Serial's resistance on CMD / DAT0~7 line	SR_{CMD} $SR_{DAT0\sim7}$	0	47	0	ohm	
V_{CCQ} decoupling capacitor		2.2+0.1	10+0.22	2.2+0.1	µF	It should be located as close as possible to the balls defined in order to minimize connection parasitic
	CH1	1	2.2	1		CH1 is only for HS200. It should be placed adjacent to VCCQ-VSSQ balls (#K6 and #K4 accordingly, next to DAT [7..0] balls). It should be located as close as possible to the balls defined in order to minimize connection parasitic.
V_{CC} capacitor value		2.2+0.1	10+0.22	4.7+0.1	µF	It should be located as close as possible to the balls defined in order to minimize connection parasitic
V_{DDi} capacitor value		1+0.1	2.2+0.1	1+0.1	µF	To stabilize regulator output to controller core logics. It should be located as close as possible to the balls defined in order to minimize connection parasitic

Table 12– Signal Line Load

7.2.4 HS400 reference load

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The circuit in Figure 10 shows the reference load used to define the HS400 Device Output Timings and overshoot / undershoot parameters.

The reference load is made up by the transmission line and the CREFERENCE capacitance.

The reference load is not intended to be a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester.

System designers should use IBIS or other simulation tools to correlate the reference load to system environment. Manufacturers should correlate to their production test conditions.

Delay time (td) of the transmission line has been introduced to make the reference load independent from the PCB technology and trace length.

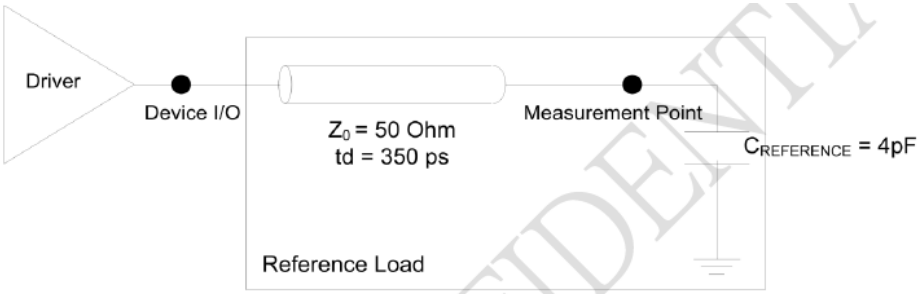

Figure 11 – HS400 reference load

7.3 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

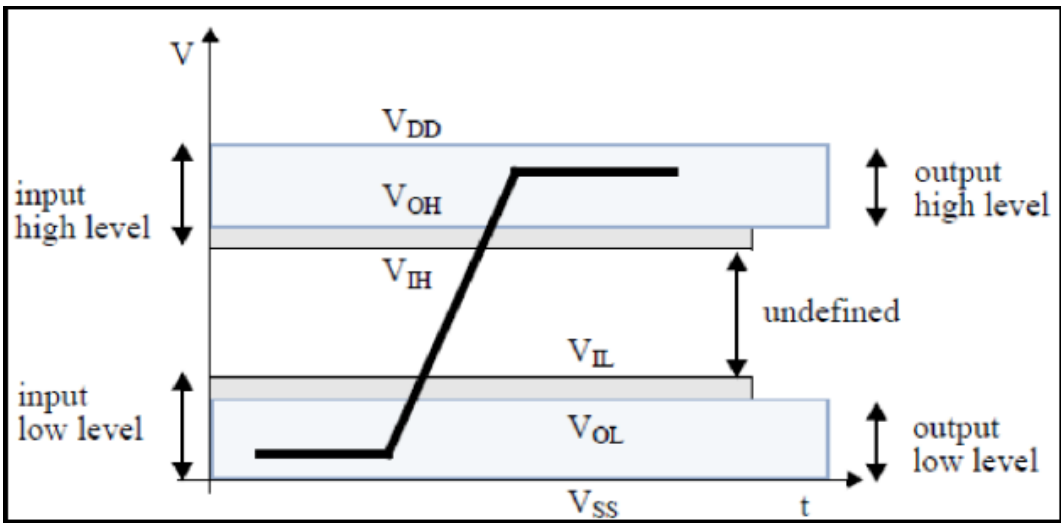

Figure 12 – Bus Signal Levels

7.3.1 Open-drain Mode Bus Signal Level

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	VOH	VDD – 0.2		V	IOH = -100 µA
Output LOW voltage	VOL		0.3	V	IOL = 2 mA

Table 13– Open-drain Bus Signal Level

The input levels are identical with the push-pull mode bus signal levels.

7.3.2 Push-pull mode bus signal level— eMMC

The device input and output voltages shall be within the following specified ranges for any VDD of the allowed voltage range

For 2.7V-3.6V VCCQ range (compatible with JESD8C.01)

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	VOH	0.75 * VCCQ		V	IOH = -100 µA @ V_{CCQ} min
Output LOW voltage	VOL		0.125 * VCCQ	V	IOL = 100 µA @ V_{CCQ} min
Input HIGH voltage	VIH	0.625 * VCCQ	VCCQ + 0.3	V	
Input LOW voltage	VIL	VSS – 0.3	0.25 * VCCQ	V	

Table 14– Push-pull Signal Level—High-voltage eMMC

For 1.70V – 1.95V VCCQ range (: Compatible with EIA/JEDEC Standard “EIA/JESD8-7 Normal Range” as defined in the following table.

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	VOH	V_{CCQ} – 0.45V		V	IOH = -2mA
Output LOW voltage	VOL		0.45V	V	IOL = 2mA
Input HIGH voltage	VIH	0.65 * V_{CCQ} [1]	V_{CCQ} + 0.3	V	
Input LOW voltage	VIL	V_{SS} – 0.3	0.35 * V_{DD} [2]	V	
Note1：0.7 * V_{DD} for MMC™4.3 and older revisions. Note2：0.3 * V_{DD} for MMC™4.3 and older revisions.					

Table 15– Push-pull Signal Level—1.70 -1.95 VCCQ Voltage Range

7.3.3 Bus Operating Conditions for HS200 & HS400

The bus operating conditions for HS200 devices is the same as specified in sections 10.5.1 of JESD84-B51 through 10.5.2 of JESD84-B51. The only exception is that VCCQ=3.3v is not supported.

7.3.4 Device Output Driver Requirements for HS200 & HS400

Refer to section 10.5.4 of the JEDEC Standard Specification No.JESD84-B51.

7.4 Bus Timing

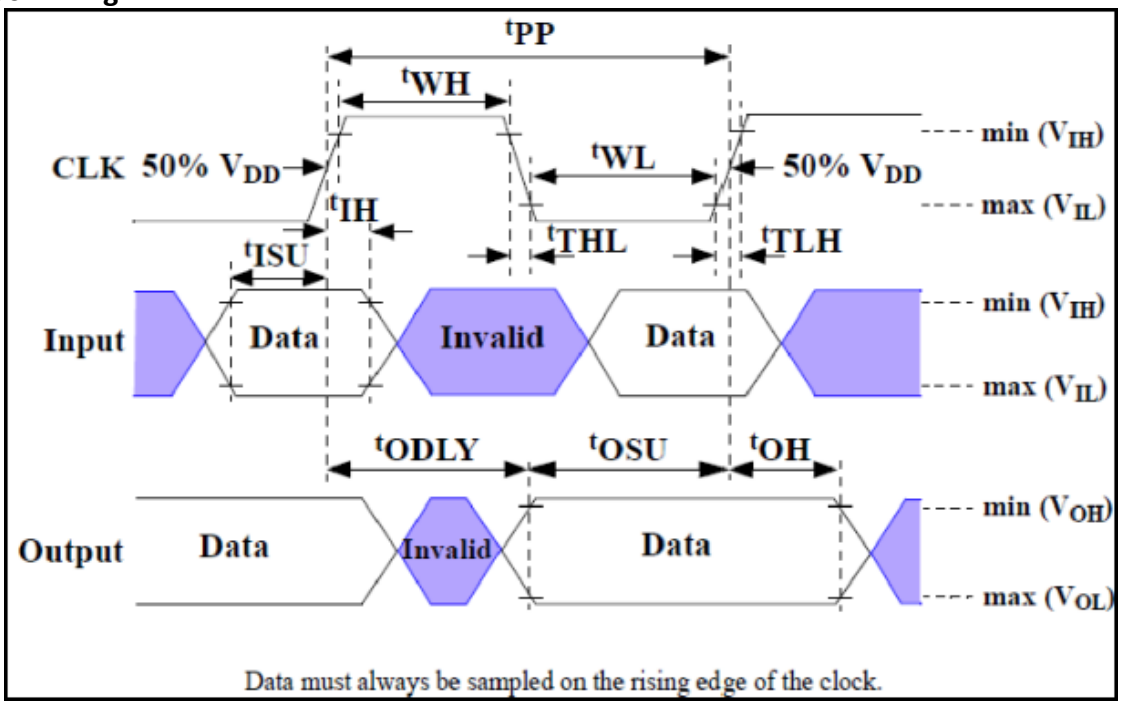

Figure 13– Timing Diagram

7.4.1 Device Interface Timings

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK[1]					
Clock frequency Data Transfer Mode (PP)[2]	fPP	0	52[3]	MHz	CL ≤ 30 pF Tolerance:+100KHz
Clock frequency Identification Mode (OD)	fOD	0	400	kHz	Tolerance: +20KHz
Clock high time	tWH	6.5		ns	CL ≤ 30 pF
Clock low time	tWL	6.5		ns	CL ≤ 30 pF
Clock rise time[4]	tTLH		3	ns	CL ≤ 30 pF
Clock fall time	tTHL		3	ns	CL ≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	3		ns	CL ≤ 30 pF
Input hold time	tIH	3		ns	CL ≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	tODLY		13.7	ns	CL ≤ 30 pF
Output hold time	tOH	2.5		ns	CL ≤ 30 pF
Signal rise time[5]	tRISE		3	ns	CL ≤ 30 pF

Note1：CLK timing is measured at 50% of VDD.
Note2： *eMMC* shall support the full frequency range from 0-26Mhz or 0-52MHz
Note3：Device can operate as high-speed Device interface timing at 26 MHz clock frequency.
Note4：CLK rise and fall times are measured by min (VIH) and max (VIL).
Note5：Inputs CMD DAT rise and fall times are measured by min (VIH) and max (VIL) and outputs CMD DAT rise and fall times are measured by min (VOH) and max (VOL). "

Table 16– High-speed Device Interface Timing

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Parameter	Symbol	Min	Max.	Unit	Remark[1]
Clock CLK[2]					
Clock frequency Data Transfer Mode (PP)[3]	fPP	0	26	MHz	CL ≤ 30 pF
Clock frequency Identification Mode (OD)	fOD	0	400	kHz	
Clock high time	tWH	10			CL ≤ 30 pF
Clock low time	tWL	10		ns	CL ≤ 30 pF
Clock rise time[4]	tTLH		10	ns	CL ≤ 30 pF
Clock fall time	tTHL		10	ns	CL ≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	3		ns	CL ≤ 30 pF
Input hold time	tIH	3		ns	CL ≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output hold time[5]	tOH	8.3		ns	CL ≤ 30 pF

Note1：The Device must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.

Note2：CLK timing is measured at 50% of VDD.

Note3：For compatibility with Devices that support the v4.2 standard or earlier, host should not use > 26 MHz before switching to high-speed interface timing.

Note4：CLK rise and fall times are measured by min (VIH) and max (VIL).

Note5：tOSU and tOH are defined as values from clock rising edge. However, there may be Devices or devices which utilize clock falling edge to output data in backward compatibility mode. Therefore, it is recommended for hosts either to settWL value as long as possible within the range which will not go over tCK-tOH(min) in the system or to use slow clock frequency, so that host could have data set up margin for those devices. In this case, each device which utilizes clock falling edge might show the correlation either between tWL and tOSU or between tCK and tOSU for the device in its own datasheet as a note or its application notes.

Table 17– Backward-compatible Device Interface Timing

7.5 Bus Timing for DAT Signals During Dual Data Rate Operation

These timings apply to the DAT[7:0] signals only when the device is configured for dual data mode operation. In this dual data mode, the DAT signals operate synchronously of both the rising and the falling edges of CLK. The CMD signal still operates synchronously of the rising edge of CLK and therefore complies with the bus timing specified in section 10.5, therefore there is no timing change for the CMD signal.

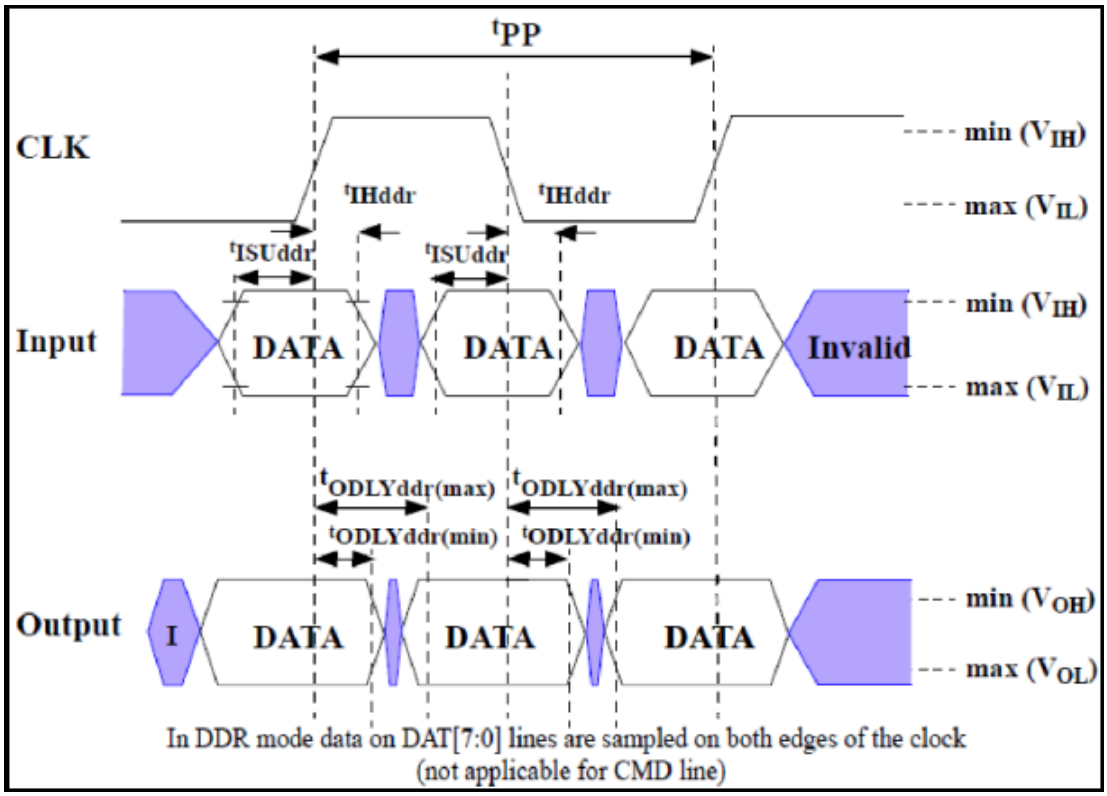


Figure14– Timing Diagram: Data Input/output in Dual Data Rate Mode

7.5.1 Dual Data Rate Interface Timings

Parameter	Symbol	Min	Max.	Unit	Remark
Input CLK[1]					
Clock duty cycle		45	55	%	Includes jitter, phase noise
Input DAT (referenced to CLK-DDR mode)					
Input set-up time	tISUddr	2.5		ns	CL ≤ 20 pF
Input hold time	tIHddr	2.5		ns	CL ≤ 20 pF
Output DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	tODLYddr	1.5	7	ns	CL ≤ 20 pF
Signal rise time (all signals)[2]	tRISE		2	ns	CL ≤ 20 pF
Signal fall time (all signals)	tFALL		2	ns	CL ≤ 20 pF
Note1：CLK timing is measured at 50% of VDD. Note2：Inputs CMD, DAT rise and fall times are measured by min (V_{IH}) and max (V_{IL}), and outputs CMD, DAT rise and fall times are measured by min (V_{OH}) and max (V_{OL})					

Table 18– High-speed Dual Data Rate Interface Timing

7.6 Bus Timing Specification in HS200 Mode

7.6.1 HS200 Clock Timing

Host CLK Timing in HS200 mode shall conform to the timing specified in Figure and Table18. CLK input shall satisfy the clock timing over all possible operation and environment conditions. CLK input parameters should be measured while CMD and DAT lines are stable high or low, as close as possible to the Device.

The maximum frequency of HS200 is 200MHz. Hosts can use any frequency up to the maximum that HS200 mode allows.

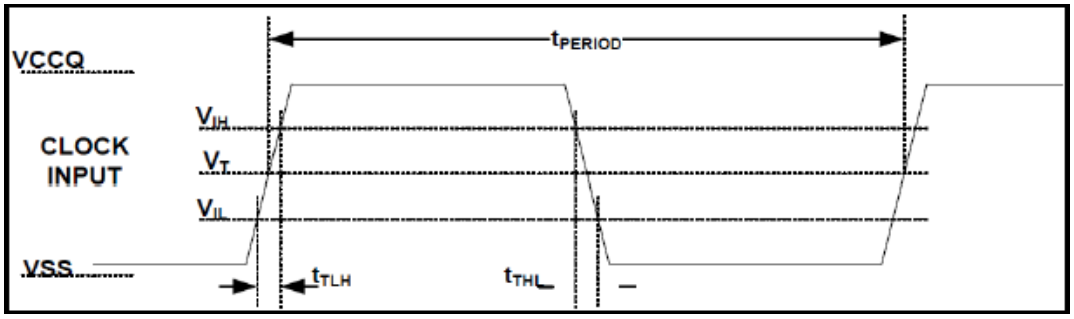


Figure 15– HS200 Clock Signal Timing

Note1：V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

Note2：VT = 50% of V_{CCQ}, indicates clock reference point for timing measurements

Symbol	Min.	Max.	Unit	Remark
t_{PERIOD}	5	-	ns	200MHz (Max.), between rising edges
t_{TLH}, t_{THL}	-	0.2* t_{PERIOD}	ns	t_{TLH}, t_{THL} < 1ns (max.) at 200MHz, C_{BGA}=12pF, The absolute maximum value of t_{TLH}, t_{THL} is 10ns regardless of clock frequency.
Duty Cycle	30	70	%	

Table 19– HS200 Clock Signal Timing

7.6.2 HS200 Device Input Timing

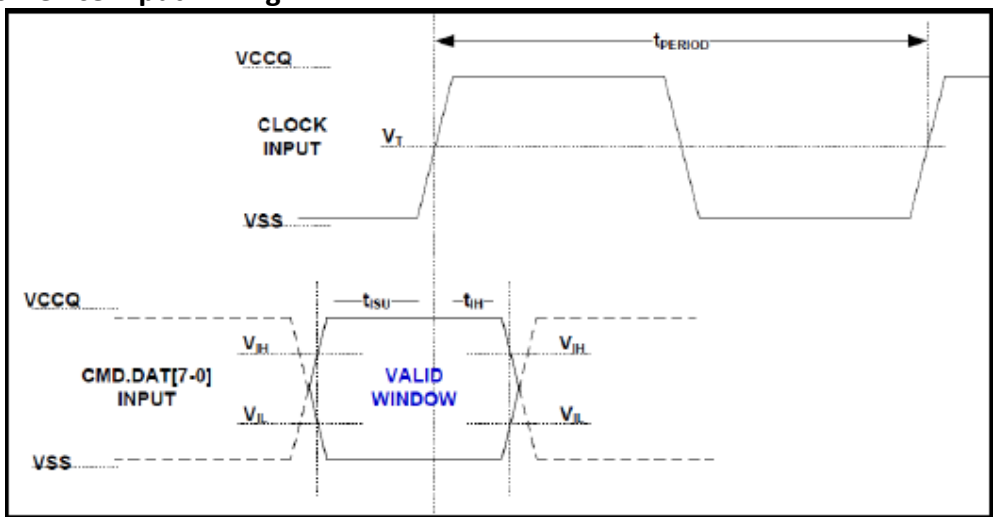


Figure 16– HS200 Device Input Timing

Note1: t_{ISU} and t_{IH} are measured at V_{IL}(max.) and VIH(min.).

Note2: VIH denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

Symbol	Min.	Max.	Unit	Remark
t_{ISU}	1.4	-	ns	$C_{BGA} \leq 6pF$
t_{IH}	0.8		ns	$C_{BGA} \leq 6pF$

Table 20 – HS200 Device Input Timing

7.6.3 HS200 Device Output Timing

tPH parameter is defined to allow device output delay to be longer than tPERIOD. After initialization, the tPH may have random phase relation to the clock. The Host is responsible to find the optimal sampling point for the Device outputs, while switching to the HS200 mode.

Figure 16 and Table 20 define Device output timing.

While setting the sampling point of data, a long term drift, which mainly depends on temperature drift, should be considered. The temperature drift is expressed by ΔTPH. Output valid data window (tVW) is available regardless of the drift (ΔT_{PH}) but position of data window varies by the drift, as described in Figure 17.

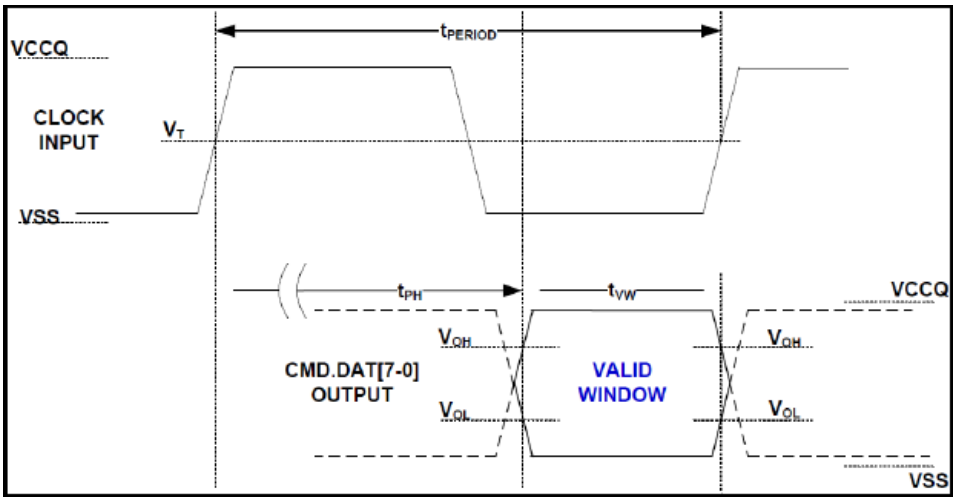


Figure 17 – HS200 Device Output Timing

Note: VOH denotes V_{OH}(min.) and V_{OL} denotes V_{OL}(max.).

Symbol	Min.	Max.	Unit	Remark
t_{PH}	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
ΔT_{PH}	-350 (ΔT=-20°C)	+1550 (ΔT=90°C)	ps	Delay variation due to temperature change after tuning. Total allowable shift of output valid window (T_{VW}) from last system Tuning procedure ΔT_{PH} is 2600ps for ΔT from -25°C to 125°C during operation.
T_{VW}	0.575	-	UI	t_{VW}=2.88ns at 200MHz Using test circuit in Figure 15 including skew among CMD and DAT lines created by the Device. Host path may add Signal Integrity induced noise, skews, etc. Expected T_{VW} at Host input is larger than 0.475UI.
Note：Unit Interval (UI) is one bit nominal time. For example, UI=5ns at 200MHz.				

Table 21– Output Timing

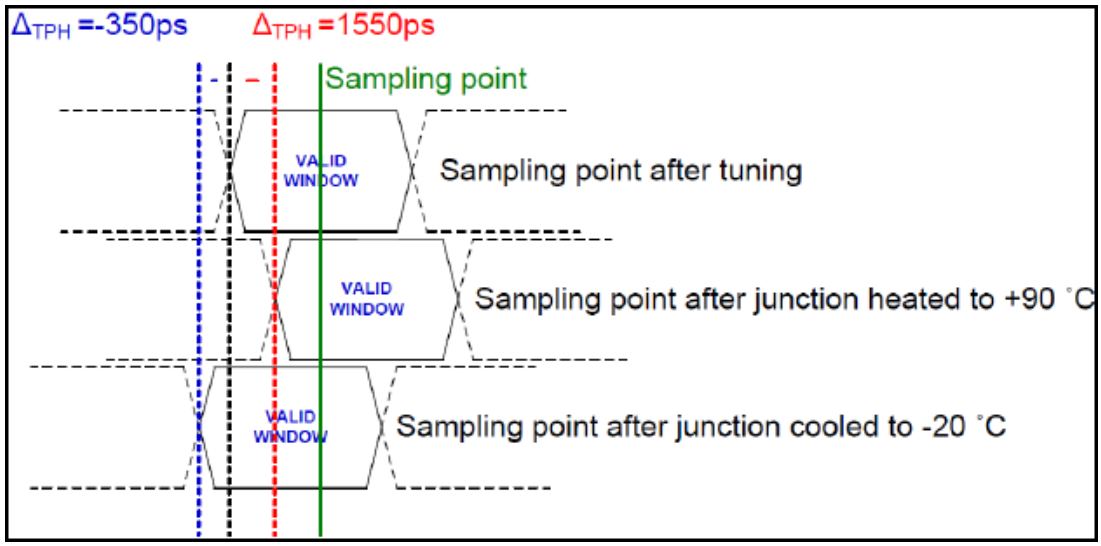


Figure 18– ΔT_{PH} consideration

Implementation Guide: Host should design to avoid sampling errors that may be caused by the Δ_{TPH} drift. It is recommended to perform tuning procedure while Device wakes up, after sleep. One simple way to overcome the Δ_{TPH} drift is by reduction of operating frequency.

7.7 Bus Timing Specification in HS400 mode

7.7.1 HS400 Device Input Timing

The CMD input timing for HS400 mode is the same as CMD input timing for HS200 mode.

Figure 18 and Table 21 show Device input timing

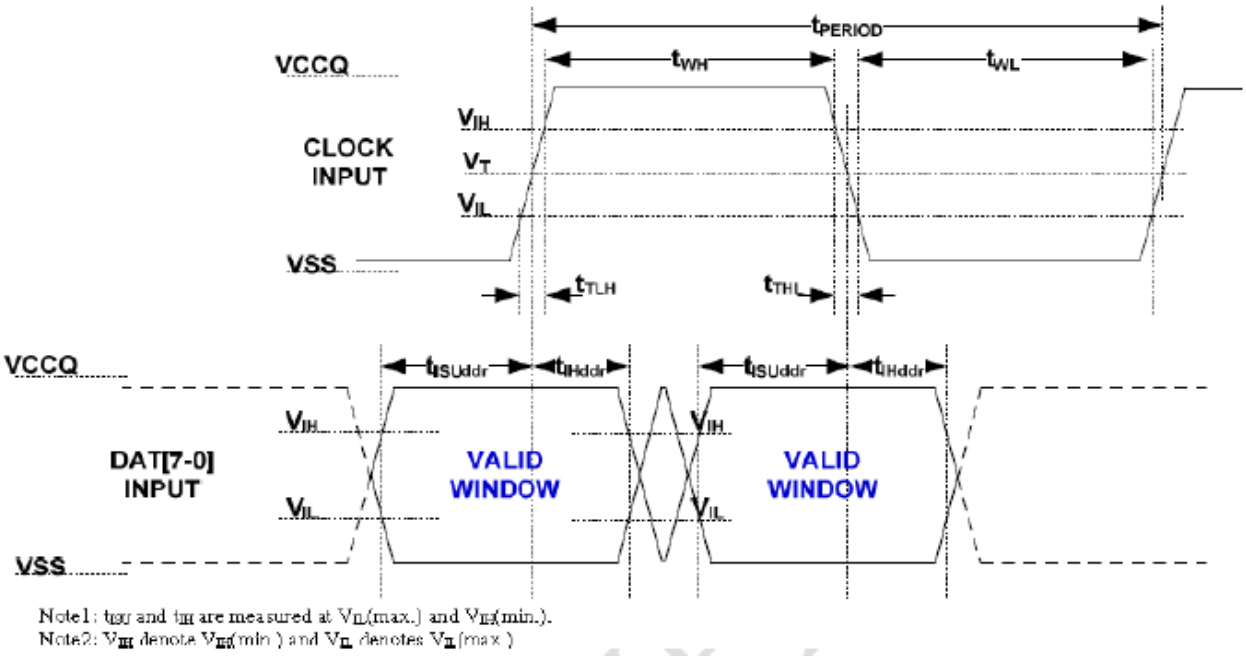


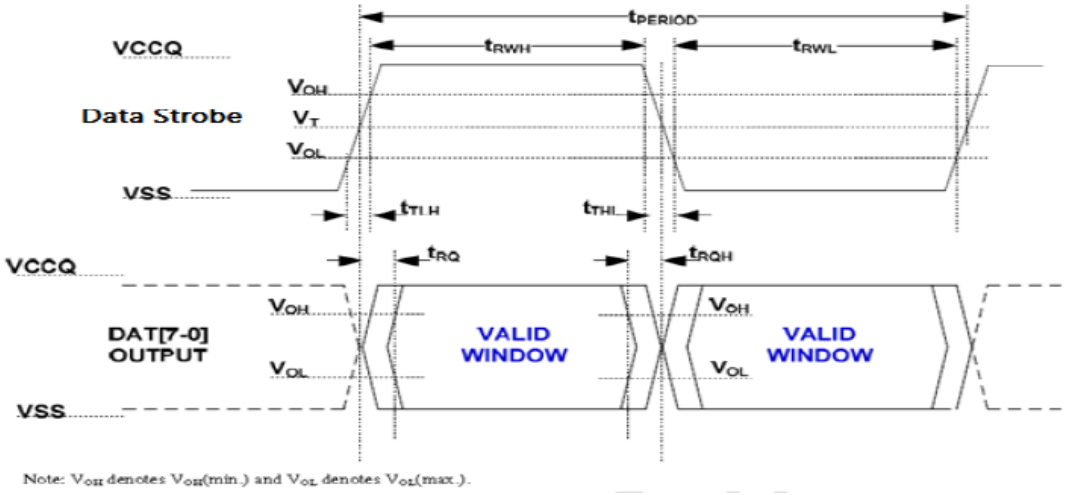
Figure 19 - HS400 Device Data input timing

Parameter	Symbol	Min	Max	Unit	Remark
Input CLK					
Cycle time data transfer mode	tPERIOD	5			200MHz(Max), between rising edges With respect to VT.
Slew rate	SR	1.125		V/ns	With respect to VIH/VIL.
Duty cycle distortion	tCKDCD	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to VT. Includes jitter, phase
Minimum pulse width	tCKMPW	2.2		ns	With respect to VT.
Input DAT (referenced to CLK)					
Input set-up time	tISUddr	0.4		ns	CDevice ≤ 6pF With respect to VIH/VIL.
Input hold time	tIHddr	0.4		ns	CDevice ≤ 6pF With respect to VIH/VIL.
Slew rate	SR	1.125		V/ns	With respect to VIH/VIL.

Table 22- HS400 Device input timing

7.7.2 HS400 Device Output Timing

The Data Strobe is used to read data in HS400 mode. The Data Strobe is toggled only during data read or CRC status response.



Note：VT = 50% of VCCQ, indicates clock reference point for timing measurements.

Figure 20- HS400 Device output timing

Parameter	Symbol	Min	Max	Unit	Remark
Data Strobe					
Cycle time data transfer mode	tPERIOD	5			200MHz(Max), between rising edges With respect to VT
Slew rate	SR	1.125		V/ns	With respect to VOH/VOL and HS400 reference load
Duty cycle distortion	tDSDCD	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion (tCKDCD) With respect to VT Includes jitter, phase noise
Minimum pulse width	tDSMPW	2.0		ns	With respect to VT
Read pre-amble	tRPRE	0.4	-	tPERIOD	Max value is specified by manufacturer. Value up to infinite is valid
Read post-amble	tRPST	0.4	-	tPERIOD	Max value is specified by manufacturer. Value up to infinite is valid
Output DAT (referenced to Data Strobe)					
Slew rate	SR	1.125		V/ns	With respect to VOH/VOL and HS400 reference load

Table 23 – HS400 Device Output timing

NOTE: Measured with HS400 reference load(6.2.4)

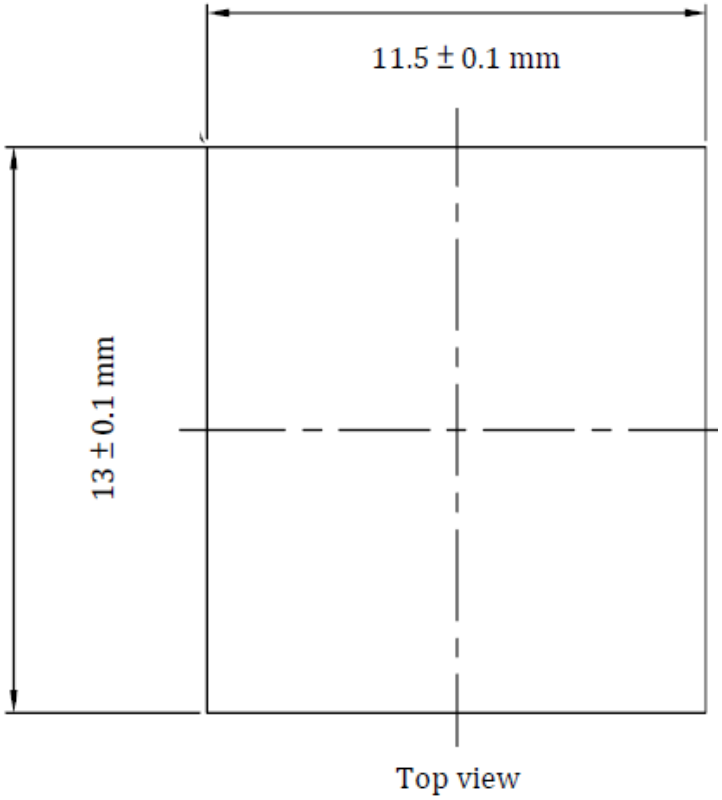
Parameter	Symbol	Min	Type	Max	Unit	Remark
Pull-up resistance for CMD	RCMD	4.7		50	Kohm	
Pull-up resistance for DAT0-7	RDAT	10		50	Kohm	
Pull-down resistance for Data Strobe	RDS	10		50	Kohm	
Internal pull up resistance DAT1-DAT7	Rint	10		150	Kohm	
Single Device capacitance	CDevice			6	pF	

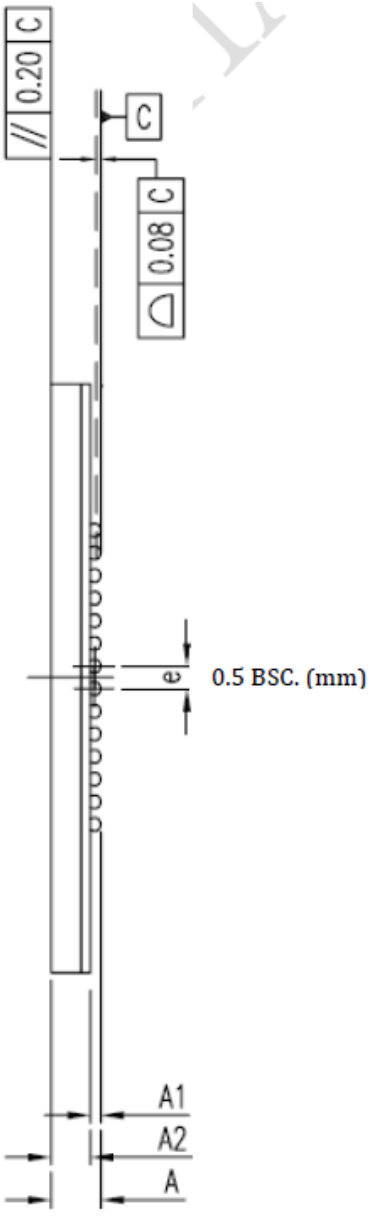
Table 24 – HS400 Capacitance

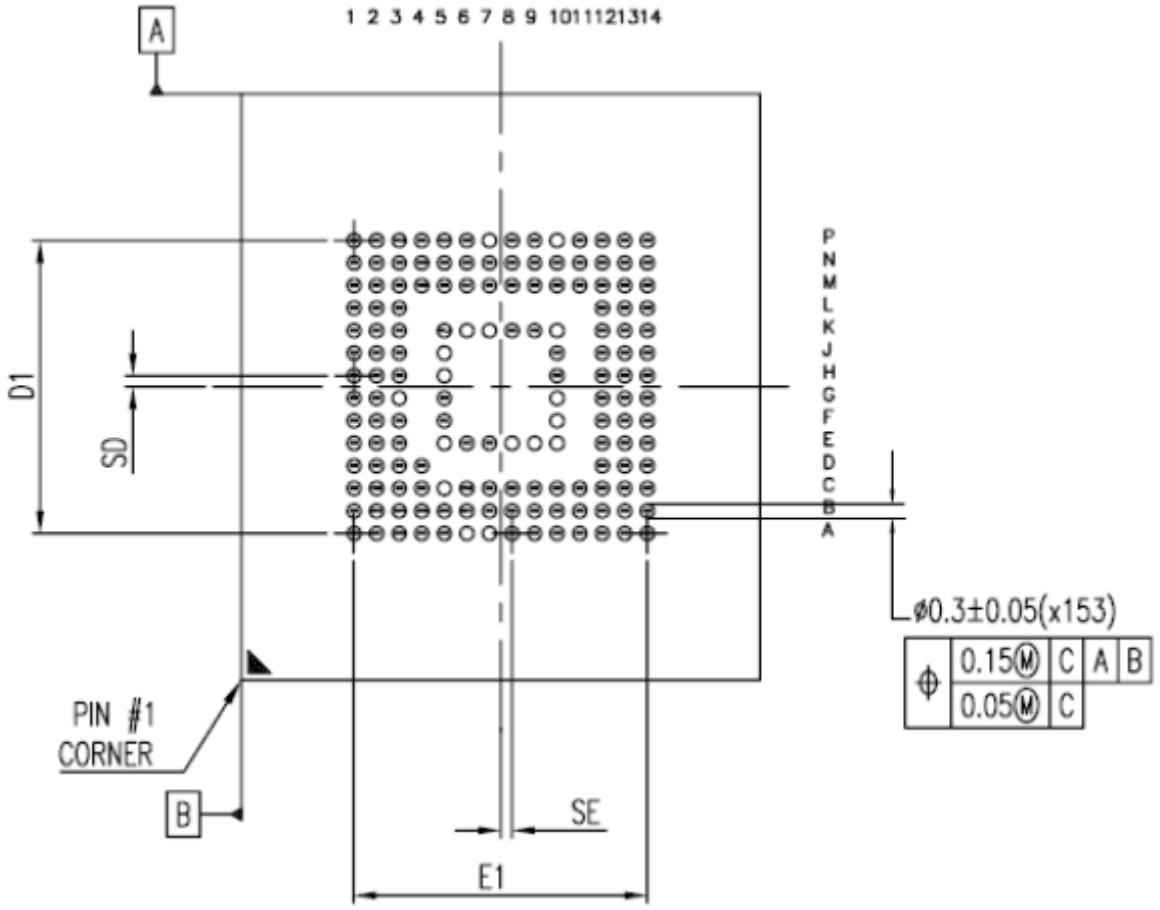
8. Package Connections

Package Mechanical (11.5 x 13.0 x 1.0mm)

A1 (Min.)	A2 (Nom.)	A (Max.)
0.16 mm	0.69 mm	1.0 mm







N	SE (MM)	SD (MM)	E1(MM)	D1(MM)	JEDEC(REF)
153	0.25 BSC.	0.25 BSC.	6.50 BSC.	6.50 BSC.	MO-276 BA

9. Ball Assignment (153 Ball)

eMMC 5.1 Ball Assignment (153 Ball)

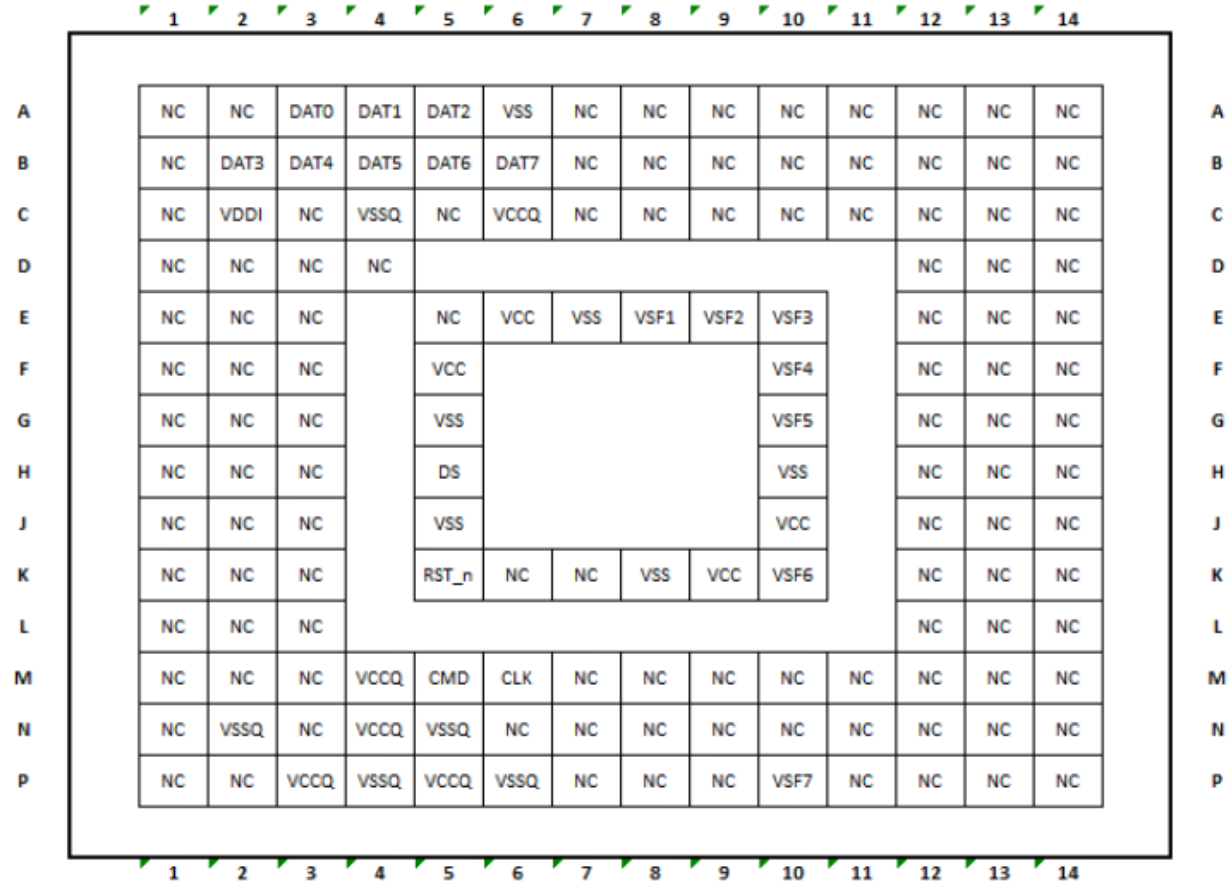
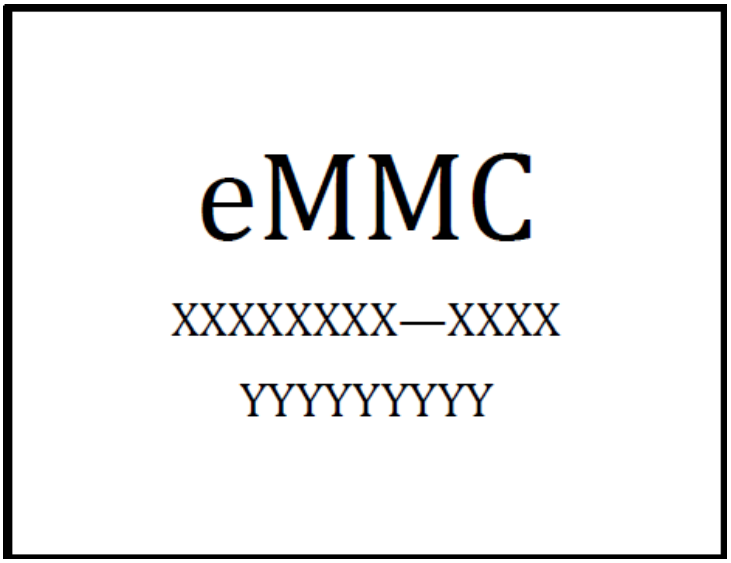


Figure 21-1 153 Ball Assignment

10. Part Number and Marking Naming Rule

eMMC logo

- XXXXXXXX-XXXX：Manufacturer part number
- YYYYYYYYY：Packaging Lots Code



11. Appendix: Part Number Table

Product	Advantech PN	Manufacture PN
SQF 153ball eMMC Industrial, 32GB, 3D TLC BiCS5, (-25-85°C)	SQF-MM5V1-32GDM9C	PTE4A0TN-32GE
SQF 153ball eMMC Industrial, 64GB, 3D TLC BiCS5, (-25-85°C)	SQF-MM5V1-64GDM9C	PTE4A0TN-64GE
SQF 153ball eMMC Industrial, 128GB, 3D TLC BiCS5, (-25-85°C)	SQF-MM5V2-128GDM9C	PTE4A0TN-X28E
SQF 153ball eMMC Industrial, 256GB, 3D TLC BiCS5, (-25-85°C)	SQF-MM5V4-256GDM9C	PTE4A0TN-X56E
SQF 153ball eMMC Industrial, 8GB, 3D sTLC BiCS5, (-25-85°C)	SQF-MM5Z1-8GDM9C	PPE4A0TN-08GE
SQF 153ball eMMC Industrial, 16GB, 3D sTLC BiCS5, (-25-85°C)	SQF-MM5Z1-16GDM9C	PPE4A0TN-16GE
SQF 153ball eMMC Industrial, 32GB, 3D sTLC BiCS5, (-25-85°C)	SQF-MM5Z1-32GDM9C	PPE4A0TN-32GE
SQF 153ball eMMC Industrial, 64GB, 3D sTLC BiCS5, (-25-85°C)	SQF-MM5Z1-64GDM9C	PPE4A0TN-64GE